CM4X16GD3200C16N2E
DDR4 DIMM OEM

Key Features

- DDR4, Vengeance RGB RT Black, 3200MHz, CAS 16, 16GB, single rank.
- 288-pin dual in-line memory module. (DIMM)
- Utilizes high performance DRAM ICs thoroughly tested for maximum interoperability and reliability.
- Base SPD settings of 2133MHz 15-15-15-36 (t_{CL}-t_{RCD}-t_{RP}-t_{RAS}), 1.2V and XMP settings of 3200MHz 16-20-20-38 (t_{CL}-t_{RCD}-t_{RP}-t_{RAS}), 1.35V.
- 100% tested at 3200MHz in a 1 DIMM per channel configuration.
- Designed for use in qualified DDR4 desktop platforms.
- Guaranteed operation 2-up. Two years warranty.
- RoHS Compliant.

Revision History

Revision	Date	Description
1.0	Jun 2023	Initial Release

Ordering Information

Part Number	CM4X16GD3200C16N2E
UPC	840006673231
Description	16GB, DDR4, UDIMM, single rank, RoHS compliant
Shipping Dimension	333mm x 203mm x 45mm
Shipping Weight	1.13 kg
Master Pack Quantity	50 modules
Master Pack Dimension	333mm x 203mm x 45mm
Master Pack Weight	1.13 kg

Notes:

1. Ordering the standard production part number allows Corsair to fulfill the order with any DRAM that has passed Corsair's rigorous internal qualification requirements for this product. If you have additional version control requirements, please contact your Corsair Sales Representative.

General Description

The CM4X16GD3200C16N2E is an 16GB DDR4 SDRAM DIMM modules. The CM4X16GD3200C16N2E is bulk packaged in a 25-unit.

The CM4X16GD3200C16N2E is verified to operate in up to 1 DIMM per channel configuration (i.e., 4-up in four channel platforms, 2-up in two channel platforms) at 3200MHz with latencies of 16-20-20-38 (t_{CAS} – t_{RCD} – t_{RP} – t_{RAS}) at 1.35V through the SPD (Serial Presence Detect) settings contained on the module.

Best of Corsair's engineering

Corsair performs rigorous testing and screening on all components to select only the best for Corsair modules. The tests check for high frequency and/or low latency capabilities for each IC. Then, they are thoroughly tested for maximum interoperability and reliability as a united group to meet the stringent design criteria demanded by performance computing and gaming users.

Pin Assignments and Descriptions

DDR4 288 Pin UDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
12V, NC	1	145	12V, NC
VSS	2	146	VREFCA
DQ4	3	147	VSS
VSS	4	148	DQ5
DQ0	5	149	VSS
VSS	6	150	DQ1
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS
TDQS9_c, DQS9_c, NC	8	152	DQS0_c
VSS	9	153	DQS0_t
DQ6	10	154	VSS
VSS	11	155	DQ7
DQ2	12	156	VSS
VSS	13	157	DQ3
DQ12	14	158	VSS
VSS	15	159	DQ13
DQ8	16	160	VSS
VSS	17	161	DQ9
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS
TDQS10_c, DQS10_c, NC	19	163	DQS1_c
VSS	20	164	DQS1_t
DQ14	21	165	VSS
VSS	22	166	DQ15
DQ10	23	167	VSS
VSS	24	168	DQ11
DQ20	25	169	VSS
VSS	26	170	DQ21
DQ16	27	171	VSS
VSS	28	172	DQ17
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS
TDQS11_c, DQS11_c, NC	30	174	DQS2_c
VSS	31	175	DQS2_t
DQ22	32	176	VSS
VSS	33	177	DQ23
DQ18	34	178	VSS
VSS	35	179	DQ19
DQ28	36	180	VSS
VSS	37	181	DQ29
DQ24	38	182	VSS
VSS	39	183	DQ25
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS
TDQS12_c, DQS12_c, NC	41	185	DQS3_c
VSS	42	186	DQS3_t
DQ30	43	187	VSS
VSS	44	188	DQ31
DQ26	45	189	VSS
VSS	46	190	DQ27
CB4, NC	47	191	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
CK0_t	74	218	CK1_t
CK0_c	75	219	CK1_c
VDD	76	220	VDD
VTT	77	221	VTT
KEY			
EVENT_n	78	222	PARITY
A0	79	223	VDD
VDD	80	224	BA1
BA0	81	225	A10/AP
RAS_n/A16	82	226	VDD
VDD	83	227	RFU
CS0_n	84	228	WE_n/A14
VDD	85	229	VDD
CAS_n/A15	86	230	NC, SAVE_n
ODT0	87	231	VDD
VDD	88	232	A13
CS1_n	89	233	VDD
VDD	90	234	NC, A17
ODT1	91	235	NC, C2
VDD	92	236	VDD
C0, CS2_n, NC	93	237	NC, CS3_n, C1
VSS	94	238	SA2
DQ36	95	239	VSS
VSS	96	240	DQ37
DQ32	97	241	VSS
VSS	98	242	DQ33
TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
TDQS13_c, DQS13_c, NC	100	244	DQS4_c
VSS	101	245	DQS4_t
DQ38	102	246	VSS
VSS	103	247	DQ39
DQ34	104	248	VSS
VSS	105	249	DQ35
DQ44	106	250	VSS
VSS	107	251	DQ45
DQ40	108	252	VSS
VSS	109	253	DQ41
TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS
TDQS14_c, DQS14_c, NC	111	255	DQS5_c
VSS	112	256	DQS5_t
DQ46	113	257	VSS
VSS	114	258	DQ47
DQ42	115	259	VSS
VSS	116	260	DQ43
DQ52	117	261	VSS
VSS	118	262	DQ53

Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	48	192	CB5, NC
CB0, NC	49	193	VSS
VSS	50	194	CB1, NC
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS
TDQS17_c, DQS17_c, NC	52	196	DQS8_c
VSS	53	197	DQS8_t
CB6, NC	54	198	VSS
VSS	55	199	CB7, NC
CB2, NC	56	200	VSS
VSS	57	201	CB3, NC
RESET_n	58	202	VSS
VDD	59	203	CKE1
CKE0	60	204	VDD
VDD	61	205	RFU
ACT_n	62	206	VDD
BG0	63	207	BG1
VDD	64	208	ALERT_n
A12/BC_n	65	209	VDD
A9	66	210	A11
VDD	67	211	A7
A8	68	212	VDD
A6	69	213	A5
VDD	70	214	A4
A3	71	215	VDD
A1	72	216	A2
VDD	73	217	VDD

Front Side Pin Label	Pin	Pin	Back side Pin Label
DQ48	119	263	VSS
VSS	120	264	DQ49
TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS15_c, DQS15_c, NC	122	266	DQS6_c
VSS	123	267	DQS6_t
DQ54	124	268	VSS
VSS	125	269	DQ55
DQ50	126	270	VSS
VSS	127	271	DQ51
DQ60	128	272	VSS
VSS	129	273	DQ61
DQ56	130	274	VSS
VSS	131	275	DQ57
TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
TDQS16_c, DQS16_c, NC	133	277	DQS7_c
VSS	134	278	DQS7_t
DQ62	135	279	VSS
VSS	136	280	DQ63
DQ58	137	281	VSS
VSS	138	282	DQ59
SA0	139	283	VSS
SA1	140	284	VDDSPD
SCL	141	285	SDA
VPP	142	286	VPP
VPP	143	287	VPP
RFU	144	288	VPP

1. Light colored text indicates functions that are not applicable for UDIMM wiring. An example is the NC for pin 234 because UDIMMs defined by this specification will never have DIMM wiring for this pin.

Pin Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is mux'ed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. TDQS is not valid for UDIMMs.
BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.

Symbol	Type	Function
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. In case of not connected as Signal, ALERT_n Pin must be connected to VDD on DIMM.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VTT[2]	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12V	Supply	12 Volt supply not used on UDIMMs.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD.
VREFCA	Supply	Reference voltage for CA

1. For PC4 VDD 1.2 V. For PC4L VDD is TBD.
2. For PC4 VTT is 0.60 V. For PC4L VTT is TBD.

Electrical Specifications

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE 1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only
and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE 1 Under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
NOTE 3 DC bandwidth is limited to 20MHz.

Differential AC and DC Input Levels

All voltages are referenced to V_{SS}

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
V_{IHdiff}	differential input high	TBD	NOTE 3	TBD	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	TBD	NOTE 3	TBD	V	1
$V_{IHdiff}(AC)$	differential input high ac	2 x ($V_{IH}(AC)$ - V_{REF})	NOTE 3	2 x ($V_{IH}(AC)$ - V_{REF})	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	2 x ($V_{IL}(AC)$ - V_{REF})	NOTE 3	2 x ($V_{IL}(AC)$ - V_{REF})	V	2

NOTE 1 Used to define a differential signal slew-rate.
NOTE 2 for CK_t - CK_c use $V_{IH}/V_{IL}(AC)$ of ADD/CMD and V_{REFCA};
NOTE 3 These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$min) for single-ended signals as well as the limitations for overshoot and undershoot.

SPD Data

Listed below is data contained in the SPD EEPROM of the CM4X16GD3200C16N2E

SPD Byte	Description	Decimal Equiv	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	35	23
1	SPD Revision	16	10
2	Key Byte / Memory Type	12	0C
3	Key Byte / Module Type	2	02
4	SDRAM Density and Banks	134	86
5	SDRAM Addressing	41	29
6	SDRAM Device Type	0	00
7	SDRAM Optional Features	8	08
8	SDRAM Thermal and Refresh Options	0	00
9	Reserved	0	00
10	Reserved	0	00
11	Module Nominal Voltage, VDD	3	03
12	Module Organization	1	01
13	Module Memory Bus Width	3	03
14	Module Thermal Sensor	0	00
15	Reserved	0	00
16	Reserved	0	00
17	Timebases	0	00
18	SDRAM Minimum Cycle Time ($t_{CKAVGmin}$)	8	08
19	SDRAM Maximum Cycle Time ($t_{CKAVGmax}$)	12	0C
20	CAS Latencies Supported, First Byte	255	FF
21	CAS Latencies Supported, Second Byte	255	FF
22	CAS Latencies Supported, Third Byte	3	03
23	CAS Latencies Supported, Fourth Byte	0	00
24	Minimum CAS Latency Time (t_{AAmin})	108	6C
25	Minimum RAS to CAS Delay Time (t_{RCDmin})	108	6C
26	Minimum Row Precharge Delay Time (t_{RPmin})	108	6C
27	Upper Nibbles for t_{RASmin} and t_{RCmin}	17	11
28	Minimum Active to Precharge Delay Time (t_{RASmin}), Least Significant Byte	8	08
29	Minimum Active to Active/Refresh Delay Time (t_{RCmin}), Least Significant Byte	116	74
30	Minimum Refresh Recovery Delay Time ($t_{RFC1min}$), LSB	48	30

31	Minimum Refresh Recovery Delay Time ($t_{RFC1min}$), MSB	17	11
32	Minimum Refresh Recovery Delay Time ($t_{RFC2min}$), LSB	240	F0
33	Minimum Refresh Recovery Delay Time ($t_{RFC2min}$), MSB	10	0A
34	Minimum Refresh Recovery Delay Time ($t_{RFC4min}$), LSB	32	20
35	Minimum Refresh Recovery Delay Time ($t_{RFC4min}$), MSB	8	08
36	Minimum Four Activate Window Time (t_{FAWmin}), Most Significant Nibble	0	00
37	Minimum Four Activate Window Time (t_{FAWmin}), Least Significant Byte	168	A8
38	Minimum Activate to Activate Delay Time (t_{RRD_Smin}), different bank group	30	1E
39	Minimum Activate to Activate Delay Time (t_{RRD_Lmin}), same bank group	43	2B
40	Minimum CAS to CAS Delay Time (t_{CCD_Lmin}), same bank group	43	2B
41	Reserved	0	00
42	Reserved	0	00
43	Reserved	0	00
44	Reserved	0	00
45	Reserved	0	00
46	Reserved	0	00
47	Reserved	0	00
48	Reserved	0	00
49	Reserved	0	00
50	Reserved	0	00
51	Reserved	0	00
52	Reserved	0	00
53	Reserved	0	00
54	Reserved	0	00
55	Reserved	0	00
56	Reserved	0	00
57	Reserved	0	00
58	Reserved	0	00
59	Reserved	0	00
60	Connector to SRAM Bit Mapping	22	16
61	Connector to SRAM Bit Mapping	54	36
62	Connector to SRAM Bit Mapping	22	16
63	Connector to SRAM Bit Mapping	54	36
64	Connector to SRAM Bit Mapping	22	16
65	Connector to SRAM Bit Mapping	54	36
66	Connector to SRAM Bit Mapping	22	16

67	Connector to SRAM Bit Mapping	54	36
68	Connector to SRAM Bit Mapping	0	00
69	Connector to SRAM Bit Mapping	0	00
70	Connector to SRAM Bit Mapping	43	2B
71	Connector to SRAM Bit Mapping	12	0C
72	Connector to SRAM Bit Mapping	43	2B
73	Connector to SRAM Bit Mapping	12	0C
74	Connector to SRAM Bit Mapping	43	2B
75	Connector to SRAM Bit Mapping	12	0C
76	Connector to SRAM Bit Mapping	43	2B
77	Connector to SRAM Bit Mapping	12	0C
78	Reserved	0	00
79	Reserved	0	00
80	Reserved	0	00
81	Reserved	0	00
82	Reserved	0	00
83	Reserved	0	00
84	Reserved	0	00
85	Reserved	0	00
86	Reserved	0	00
87	Reserved	0	00
88	Reserved	0	00
89	Reserved	0	00
90	Reserved	0	00
91	Reserved	0	00
92	Reserved	0	00
93	Reserved	0	00
94	Reserved	0	00
95	Reserved	0	00
96	Reserved	0	00
97	Reserved	0	00
98	Reserved	0	00
99	Reserved	0	00
100	Reserved	0	00
101	Reserved	0	00
102	Reserved	0	00

103	Reserved	0	00
104	Reserved	0	00
105	Reserved	0	00
106	Reserved	0	00
107	Reserved	0	00
108	Reserved	0	00
109	Reserved	0	00
110	Reserved	0	00
111	Reserved	0	00
112	Reserved	0	00
113	Reserved	0	00
114	Reserved	0	00
115	Reserved	0	00
116	Reserved	0	00
117	Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_Lmin}), same bank group	237	ED
118	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_Lmin}), same bank group	181	B5
119	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_Smin}), different bank group	206	CE
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (t_{RCmin})	0	00
121	Fine Offset for Minimum Row Precharge Delay Time (t_{RPmin})	0	00
122	Fine Offset for Minimum RAS to CAS Delay Time (t_{RCDmin})	0	00
123	Fine Offset for Minimum CAS Latency Time (t_{AAmin})	0	00
124	Fine Offset for SDRAM Maximum Cycle Time ($t_{CKAVGmax}$)	0	00
125	Fine Offset for SDRAM Minimum Cycle Time ($t_{CKAVGmin}$)	194	C2
126	CRC for Base Configuration Section, Least Significant Byte	124	7C
127	CRC for Base Configuration Section, Most Significant Byte	75	4B
128	Raw Card Extension, Module Nominal Height	17	11
129	Module Maximum Thickness	17	11
130	Reference Raw Card Used	0	00
131	Address Mapping from Edge Connector to DRAM	0	00
132	Reserved	0	00
133	Reserved	0	00
134	Reserved	0	00
135	Reserved	0	00
136	Reserved	0	00
137	Reserved	0	00

138	Reserved	0	00
139	Reserved	0	00
140	Reserved	0	00
141	Reserved	0	00
142	Reserved	0	00
143	Reserved	0	00
144	Reserved	0	00
145	Reserved	0	00
146	Reserved	0	00
147	Reserved	0	00
148	Reserved	0	00
149	Reserved	0	00
150	Reserved	0	00
151	Reserved	0	00
152	Reserved	0	00
153	Reserved	0	00
154	Reserved	0	00
155	Reserved	0	00
156	Reserved	0	00
157	Reserved	0	00
158	Reserved	0	00
159	Reserved	0	00
160	Reserved	0	00
161	Reserved	0	00
162	Reserved	0	00
163	Reserved	0	00
164	Reserved	0	00
165	Reserved	0	00
166	Reserved	0	00
167	Reserved	0	00
168	Reserved	0	00
169	Reserved	0	00
170	Reserved	0	00
171	Reserved	0	00
172	Reserved	0	00
173	Reserved	0	00

174	Reserved	0	00
175	Reserved	0	00
176	Reserved	0	00
177	Reserved	0	00
178	Reserved	0	00
179	Reserved	0	00
180	Reserved	0	00
181	Reserved	0	00
182	Reserved	0	00
183	Reserved	0	00
184	Reserved	0	00
185	Reserved	0	00
186	Reserved	0	00
187	Reserved	0	00
188	Reserved	0	00
189	Reserved	0	00
190	Reserved	0	00
191	Reserved	0	00
192	Reserved	0	00
193	Reserved	0	00
194	Reserved	0	00
195	Reserved	0	00
196	Reserved	0	00
197	Reserved	0	00
198	Reserved	0	00
199	Reserved	0	00
200	Reserved	0	00
201	Reserved	0	00
202	Reserved	0	00
203	Reserved	0	00
204	Reserved	0	00
205	Reserved	0	00
206	Reserved	0	00
207	Reserved	0	00
208	Reserved	0	00
209	Reserved	0	00

210	Reserved	0	00
211	Reserved	0	00
212	Reserved	0	00
213	Reserved	0	00
214	Reserved	0	00
215	Reserved	0	00
216	Reserved	0	00
217	Reserved	0	00
218	Reserved	0	00
219	Reserved	0	00
220	Reserved	0	00
221	Reserved	0	00
222	Reserved	0	00
223	Reserved	0	00
224	Reserved	0	00
225	Reserved	0	00
226	Reserved	0	00
227	Reserved	0	00
228	Reserved	0	00
229	Reserved	0	00
230	Reserved	0	00
231	Reserved	0	00
232	Reserved	0	00
233	Reserved	0	00
234	Reserved	0	00
235	Reserved	0	00
236	Reserved	0	00
237	Reserved	0	00
238	Reserved	0	00
239	Reserved	0	00
240	Reserved	0	00
241	Reserved	0	00
242	Reserved	0	00
243	Reserved	0	00
244	Reserved	0	00
245	Reserved	0	00

246	Reserved	0	00
247	Reserved	0	00
248	Reserved	0	00
249	Reserved	0	00
250	Reserved	0	00
251	Reserved	0	00
252	Reserved	0	00
253	Reserved	0	00
254	CRC for Module Specific Section, LSB	182	B6
255	CRC for Module Specific Section, MSB	88	58
256	Reserved	0	00
257	Reserved	0	00
258	Reserved	0	00
259	Reserved	0	00
260	Reserved	0	00
261	Reserved	0	00
262	Reserved	0	00
263	Reserved	0	00
264	Reserved	0	00
265	Reserved	0	00
266	Reserved	0	00
267	Reserved	0	00
268	Reserved	0	00
269	Reserved	0	00
270	Reserved	0	00
271	Reserved	0	00
272	Reserved	0	00
273	Reserved	0	00
274	Reserved	0	00
275	Reserved	0	00
276	Reserved	0	00
277	Reserved	0	00
278	Reserved	0	00
279	Reserved	0	00
280	Reserved	0	00
281	Reserved	0	00

282	Reserved	0	00
283	Reserved	0	00
284	Reserved	0	00
285	Reserved	0	00
286	Reserved	0	00
287	Reserved	0	00
288	Reserved	0	00
289	Reserved	0	00
290	Reserved	0	00
291	Reserved	0	00
292	Reserved	0	00
293	Reserved	0	00
294	Reserved	0	00
295	Reserved	0	00
296	Reserved	0	00
297	Reserved	0	00
298	Reserved	0	00
299	Reserved	0	00
300	Reserved	0	00
301	Reserved	0	00
302	Reserved	0	00
303	Reserved	0	00
304	Reserved	0	00
305	Reserved	0	00
306	Reserved	0	00
307	Reserved	0	00
308	Reserved	0	00
309	Reserved	0	00
310	Reserved	0	00
311	Reserved	0	00
312	Reserved	0	00
313	Reserved	0	00
314	Reserved	0	00
315	Reserved	0	00
316	Reserved	0	00
317	Reserved	0	00

318	Reserved	0	00
319	Reserved	0	00
320	Module Manufacturer ID Code, LSB	2	02
321	Module Manufacturer ID Code, MSB	158	9E
322	Module Manufacturing Location	0	00
323	Module Manufacturing Date	0	00
324	Module Manufacturing Date	0	00
325	Module Serial Number	0	00
326	Module Serial Number	0	00
327	Module Serial Number	0	00
328	Module Serial Number	0	00
329	Module Part Number	67	43
330	Module Part Number	77	4D
331	Module Part Number	52	34
332	Module Part Number	88	58
333	Module Part Number	49	31
334	Module Part Number	54	36
335	Module Part Number	71	47
336	Module Part Number	68	44
337	Module Part Number	51	33
338	Module Part Number	50	32
339	Module Part Number	48	30
340	Module Part Number	48	30
341	Module Part Number	67	43
342	Module Part Number	49	31
343	Module Part Number	54	36
344	Module Part Number	78	4E
345	Module Part Number	50	32
346	Module Part Number	69	45
347	Module Part Number	0	00
348	Module Part Number	0	00
349	Module Revision Code	0	00
350	DRAM Manufacturer ID Code, LSB	0	00
351	DRAM Manufacturer ID Code, MSB	0	00
352	DRAM Stepping	0	00
353	Module Manufacturer Specific Data	0	00

354	Module Manufacturer Specific Data	0	00
355	Module Manufacturer Specific Data	0	00
356	Module Manufacturer Specific Data	0	00
357	Module Manufacturer Specific Data	0	00
358	Module Manufacturer Specific Data	0	00
359	Module Manufacturer Specific Data	0	00
360	Module Manufacturer Specific Data	0	00
361	Module Manufacturer Specific Data	0	00
362	Module Manufacturer Specific Data	0	00
363	Module Manufacturer Specific Data	0	00
364	Module Manufacturer Specific Data	0	00
365	Module Manufacturer Specific Data	0	00
366	Module Manufacturer Specific Data	0	00
367	Module Manufacturer Specific Data	0	00
368	Module Manufacturer Specific Data	0	00
369	Module Manufacturer Specific Data	0	00
370	Module Manufacturer Specific Data	0	00
371	Module Manufacturer Specific Data	0	00
372	Module Manufacturer Specific Data	0	00
373	Module Manufacturer Specific Data	0	00
374	Module Manufacturer Specific Data	0	00
375	Module Manufacturer Specific Data	0	00
376	Module Manufacturer Specific Data	0	00
377	Module Manufacturer Specific Data	0	00
378	Module Manufacturer Specific Data	0	00
379	Module Manufacturer Specific Data	0	00
380	Module Manufacturer Specific Data	0	00
381	Module Manufacturer Specific Data	0	00
382	CRC for Manufacturing Section, LSB	0	00
383	CRC for Manufacturing Section, MSB	0	00
384	End User Programmable	12	0C
385	End User Programmable	74	4A
386	End User Programmable	1	01
387	End User Programmable	32	20
388	End User Programmable	0	00
389	End User Programmable	0	00

390	End User Programmable	0	00
391	End User Programmable	0	00
392	End User Programmable	0	00
393	End User Programmable	163	A3
394	End User Programmable	0	00
395	End User Programmable	0	00
396	End User Programmable	5	05
397	End User Programmable	255	FF
398	End User Programmable	255	FF
399	End User Programmable	3	03
400	End User Programmable	0	00
401	End User Programmable	80	50
402	End User Programmable	100	64
403	End User Programmable	100	64
404	End User Programmable	16	10
405	End User Programmable	189	BD
406	End User Programmable	34	22
407	End User Programmable	48	30
408	End User Programmable	17	11
409	End User Programmable	240	F0
410	End User Programmable	10	0A
411	End User Programmable	32	20
412	End User Programmable	8	08
413	End User Programmable	0	00
414	End User Programmable	176	B0
415	End User Programmable	30	1E
416	End User Programmable	45	2D
417	End User Programmable	0	00
418	End User Programmable	0	00
419	End User Programmable	0	00
420	End User Programmable	0	00
421	End User Programmable	0	00
422	End User Programmable	0	00
423	End User Programmable	0	00
424	End User Programmable	0	00
425	End User Programmable	0	00

426	End User Programmable	0	00
427	End User Programmable	246	F6
428	End User Programmable	246	F6
429	End User Programmable	246	F6
430	End User Programmable	246	F6
431	End User Programmable	0	00
432	End User Programmable	0	00
433	End User Programmable	0	00
434	End User Programmable	0	00
435	End User Programmable	0	00
436	End User Programmable	0	00
437	End User Programmable	0	00
438	End User Programmable	0	00
439	End User Programmable	0	00
440	End User Programmable	0	00
441	End User Programmable	0	00
442	End User Programmable	0	00
443	End User Programmable	0	00
444	End User Programmable	0	00
445	End User Programmable	0	00
446	End User Programmable	0	00
447	End User Programmable	0	00
448	End User Programmable	0	00
449	End User Programmable	0	00
450	End User Programmable	0	00
451	End User Programmable	0	00
452	End User Programmable	0	00
453	End User Programmable	0	00
454	End User Programmable	0	00
455	End User Programmable	0	00
456	End User Programmable	0	00
457	End User Programmable	0	00
458	End User Programmable	0	00
459	End User Programmable	0	00
460	End User Programmable	0	00
461	End User Programmable	0	00

462	End User Programmable	0	00
463	End User Programmable	0	00
464	End User Programmable	0	00
465	End User Programmable	0	00
466	End User Programmable	0	00
467	End User Programmable	0	00
468	End User Programmable	0	00
469	End User Programmable	0	00
470	End User Programmable	0	00
471	End User Programmable	0	00
472	End User Programmable	0	00
473	End User Programmable	0	00
474	End User Programmable	0	00
475	End User Programmable	0	00
476	End User Programmable	0	00
477	End User Programmable	0	00
478	End User Programmable	0	00
479	End User Programmable	0	00
480	End User Programmable	0	00
481	End User Programmable	0	00
482	End User Programmable	0	00
483	End User Programmable	0	00
484	End User Programmable	0	00
485	End User Programmable	0	00
486	End User Programmable	0	00
487	End User Programmable	0	00
488	End User Programmable	0	00
489	End User Programmable	0	00
490	End User Programmable	0	00
491	End User Programmable	0	00
492	End User Programmable	0	00
493	End User Programmable	0	00
494	End User Programmable	0	00
495	End User Programmable	0	00
496	End User Programmable	0	00
497	End User Programmable	0	00

498	End User Programmable	0	00
499	End User Programmable	0	00
500	End User Programmable	0	00
501	End User Programmable	0	00
502	End User Programmable	0	00
503	End User Programmable	0	00
504	End User Programmable	0	00
505	End User Programmable	0	00
506	End User Programmable	0	00
507	End User Programmable	0	00
508	End User Programmable	0	00
509	End User Programmable	0	00
510	End User Programmable	0	00
511	End User Programmable	0	00